UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LOUIS A. LIPPINCOTT

Appeal 2006-2762
Application 09/458,370
Technology Center 2600

Decided: March 22, 2007

Before KENNETH W. HAIRSTON, JOSEPH F. RUGGIERO, and LANCE LEONARD BARRY, *Administrative Patent Judges*.

RUGGERO, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant appeal under 35 U.S.C. § 134 from a final rejection of claims 1, 4-8, 11-15, 19, 23, 25, and 28, which are all of the pending claims. Claims 2, 3, 9, 10, 16-18, 20-22, 24, 26, and 27 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

Appellant's invention relates to the implementation of a two-dimensional inverse discrete cosine transform (IDCT) function in which two one-dimensional inverse discrete transform functions (IDCT) are executed.

Claim 1 is illustrative of the invention and it reads as follows:

1. A method of implementing a two-dimensional inverse discrete cosine transform, comprising:

executing first and second one-dimensional inverse discrete cosine transforming functions in first and second separate inverse discrete cosine transforming calculators, each of the first and second functions being controlled to operate on a matrix of coefficients with both of said first and second inverse discrete cosine transforming calculators operating simultaneously in a row direction at a first time, and with both of said first and second inverse discrete cosine transforming calculators operating simultaneously in a column direction at a second time.

The prior art reference relied upon by the Examiner in rejecting the claims on appeal is:

Tanaka	US 5,268,853	Dec. 7, 1993

The Examiner rejected claims 1, 4-8, 11-15, 19, 23, 25, and 28, all of the appealed claims, under 35 U.S.C. § 102(b) as being anticipated by Tanaka.

Appellant contends that the Examiner has not shown how each of the claimed features is present in the disclosure of Tanaka so as to establish a

case of anticipation.[1] In particular, Appellant contends (Br. 8-11) that, in contrast to the claimed invention, Tanaka does not provide a disclosure of first and second inverse discrete cosine transforming calculators operating simultaneously (appealed independent claims 1 and 8) or concurrently (appealed independent claims 15 and 19) in the same direction. With respect to independent claims 23 and 25, Appellant argues (Br. 11-12), that Tanaka does not disclose a sequencer which controls both of the inverse discrete cosine transforming calculators so that they operate in the same direction.

We affirm-in-part.

ISSUES

1. Does Tanaka disclose a method of implementing a two-dimensional inverse discrete cosine transform in which first and second inverse discrete cosine transforming calculators operate simultaneously or concurrently in the same direction so as to establish a prima facie case of anticipation under 35 U.S.C. § 102(b)?
2. Does the disclosure of Tanaka anticipate under 35 U.S.C. § 102(b) claims which require that a sequencer control both first and second inverse discrete cosine transforming calculators so that they operate in the same direction.

[1] This decision considers only those arguments that Appellant submitted in the Appeal Brief. Arguments that Appellant could have made but chose not to make in the Brief are deemed to have been waived. *See* 37 C.F.R. § 41.37(c)(1) (vii)(eff. Sept. 13, 2004). *See also In re Watts*, 354 F.3d 1362, 1368, 69 USPQ2d 1453, 1458 (Fed. Cir. 2004).

FINDINGS OF FACT

The implementation of a two-dimensional inverse discrete cosine transform function disclosed and claimed by Appellant involves execution by two one-dimensional inverse discrete cosine transforming calculators (Specification 3). More particularly, as set forth in each of the appealed independent claims 1 and 8, the two one-dimensional inverse discrete cosine transforming calculators operate simultaneously in a row direction at a first time, and operate simultaneously in a column direction at a second time. Using slightly different language, appealed independent claims 15 and 19 require that the two one-dimensional inverse discrete cosine transforming calculators operate concurrently in the same direction. Independent claims 23 and 25 have no requirement of simultaneous or concurrent operation of the two transforming calculators but do require a sequencer which controls both of the transforming calculators to operate in the same direction.

Tanaka discloses an orthogonal transformation processor useful for image compression which utilizes, as illustrated in Figure 5, two one-dimensional discrete cosine transforming calculators 4 and 6 which, respectively, read to and write from memory 2 under control of sequencer 8. The transforming calculators are described as operating sequentially beginning with the calculator 4 writing to memory device 2 in the row direction. (Tanaka, col. 11, ll. 9-15). At this point, the switching circuit 18 in the sequencer 8 switches the row and column addresses and the calculator starts to read from the memory in the column direction. According to Tanaka (col. 11, ll. 22-28), "[s]ubsequently ... ," the calculator writes to the memory in the column direction. The reading and writing operations are performed in the column direction until the switching circuit again switches

the row and column addresses and the reading and writing will be performed in the row direction. (Tanaka, col. 11, ll. 33-40).

PRINCIPLE OF LAW

Anticipation is established when a single prior art reference discloses expressly or under the principles of inherency each and every limitation of the claimed invention. *Atlas Powder Co. v. IRECO Inc.*, 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1946 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

ANALYSIS

With respect to independent claims 1, 8, 15, and 19, the Examiner is correct (Answer 7-12) that the switching circuit 18 of the address generator in Tanaka operates to switch the row and column addresses of memory device 2 causing the DCT calculators 4 and 6 to perform their write and read operations in alternate row and column directions. We agree with Appellant, however, that there is no support for the Examiner's conclusion that the writing and reading are performed simultaneously or concurrently in the same direction as claimed. To the contrary, it is our view that Tanaka's disclosure supports Appellant's contention that Tanaka's DCT calculators are not operating simultaneously or concurrently in the same direction.

As described in Tanaka (col. 11, ll. 22-24), after the address generator switching circuit switches the addresses from row to column and DCT calculator 6 performs a read operation in the column direction, "[s]ubsequently ...," DCT calculator 4 performs a write operation in the

column direction. In the succeeding two sentences, Tanaka (col. 11, ll. 24-28) uses the words "Next" and "Subsequently" to describe the reading and writing operations of, respectively, the DCT calculators 6 and 4. In other words, while, for example, the illustration at Figure 10 of Tanaka shows the reading and writing operations of the DCT calculators being performed in the same column direction, there is no indication that such operations are being performed simultaneously or concurrently as claimed. The illustration in Figure 9 of Tanaka lends further support for this conclusion since, as shown, the reading and writing operations are performed in different half-cycles of the clock signal CK.

With respect to independent claims 23 and 25, we reach the opposite conclusion as to the issue of whether the Examiner has established a prima-facie case of anticipation based on Tanaka. Unlike the language of independent claims 1, 8, 15, and 19 which requires that the transforming calculators operate in the same direction simultaneously or concurrently, claims 23 and 25 have no limitations directed to the timing of the operation of the two transforming calculators. Instead, claims 23 and 25 require a sequencer which controls both of the transforming calculators to operate in the same direction.

We refer to our earlier discussion of the description of the operation of Tanaka's system which noted that, after transforming calculator 4 writes to memory 2 in the row direction, the row and column addresses are switched. After this occurs, Tanaka's transforming calculator 6 reads from the memory direction in the column direction followed by writing to the memory 2 by transforming calculator 4 in the column direction before the row and column addresses are again switched. That the reading and writing operations are

performed in the same direction, albeit not simultaneously or concurrently, is verified by the illustration in Figure 10 of Tanaka which shows both the reading and writing as being performed in the column direction.

CONCLUSION

Since all of the claim limitations are not present in the disclosure of Tanaka, the Examiner has not established a prima facie case of anticipation under 35 U.S.C. § 102(b) of independent claims 1, 8, 15, 19, as well as claims 4-7, 11-14, and 28 dependent thereon. The Examiner has established a prima facie case of anticipation that has not been successfully rebutted by Appellant with respect to claims 23 and 25 since Tanaka discloses a sequencer which controls both of first and second transforming calculators to operate in the same direction.

DECISION

The anticipation rejection of claims 1, 4-8, 11-15, 19, and 28 is reversed. The anticipation rejection of claims 23 and 25 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv)(effective September 13, 2004).

AFFIRMED-IN-PART

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